thickness of the layer of germanium, the applied electric bias, and the elevated temperature.

42. (New) The method as claimed in claim 26, wherein the at least one dielectric layer comprises a plurality of dielectric layers.

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43. (New) The method as claimed in claim 32, wherein the at least one dielectric layer comprises a plurality of dielectric layers.

## REMARKS

Currently pending claims 3-6, 8, 11-12, 14, 19-21, 26-28, 30, and 32-43 are for consideration by the Examiner. Claims 33-43 are new. Claims 12 and 20 were amended prior to the present office action response. Claims 3-6, 8, 11, 14, 19, 21, 26, 28, 30, and 32 are amended herein.

The Examiner rejected claims 3-6, 19-21, 26-28 and 32 under 35 U.S.C. §103(a) as being unpatentable over Koch et al. (U.S. 5,413,884) in view of Angelopoulos et al. (6,316,167B1) and Howe et al. (U.S. 6,210,988).

The Examiner rejected claims 8 and 30 under 35 U.S.C. §103(a) as being unpatentable over Koch et al. (U.S. 5,413,884) in view of Angelopoulos et al. (6,316,167B1) and Howe et al. (U.S. 6,210,988) as applied to claims 3-6, 19-21, 26-28 and 32 above, and further in view of Cho et al. (U.S. 6,074,930).

The Examiner rejected claims 11, 12 and 14 under 35 U.S.C. §103(a) as being unpatentable over Koch et al. (U.S. 5,413,884) in view of Angelopoulos et al. (6,316,167B1) and

Cho et al. (U.S. 6,074,930) and Howe et al. (U.S. 6,210,988).

Applicants respectfully traverse the§103(a) rejections with the following arguments.

**35 U.S.C. § 103(a)**

Applicants respectfully contend that independent claims 3, 19, 26, and 32 are not unpatentable over Koch in view of Angelopoulos and Howe, because Koch in view of Angelopoulos and Howe does not teach or suggest each and every feature of independent claims 3, 19, 26, and 32. For example, Koch in view of Angelopoulos and Howe does not teach or suggest "depositing a photo resist layer over the layer of germanium" and "exposing the photo resist layer to light and developing the exposed photo resist layer to form a photolithography image". The Examiner alleges that Koch teaches "depositing a photo resist layer (46) over the layer of metallic germanium (44), exposing and developing the photo resist layer (46) to form a photolithography image 50". Applicants contend, however, that layer 46 in Koch is not a photo resist layer as is required by claims 3, 19, 26, and 32, but is instead an electron-beam sensitive resist (see Koch, col. 5, lines 44-45). Applicants further contend that the layer 46 in Koch is not exposed to light as is required by claims 3, 19, 26, and 32, but is instead exposed to an electron beam (see Koch, col. 5, lines 26-29; 46-48).

Based on the preceding arguments, Applicants respectfully maintain that independent claims 3, 19, 26, and 32 are not unpatentable over Koch in view of Angelopoulos and Howe , and that claims 3, 19, 26, and 32 are in condition for allowance. Since claims 4-6, 8, and 33-35 depend from claim 3, Applicants contend that claims 4-6, 8, and 33-35 are likewise in condition for allowance. Since claims 20-21 and 39 depend from claim 19, Applicants contend that claims

20-21 and 39 are likewise in condition for allowance. Since claims 27-28, 30, and 40-42 depend from claim 26, Applicants contend that claims 27-28, 30, and 40-42 are likewise in condition for allowance. Since claim 43 depends from claim 32, Applicants contend that claim 43 is likewise in condition for allowance.

Applicants respectfully contend that independent claim 11 is not unpatentable over Koch in view of Angelopoulos and Cho and Howe, because Koch in view of Angelopoulos and Cho and Howe does not teach or suggest each and every feature of independent claim 11. For example, Koch in view of Angelopoulos and Cho and Howe does not teach or suggest "depositing a photo resist layer over the metallic germanium layer" and "exposing the photo resist layer to light and developing the exposed photo resist layer to form a photolithography image". The Examiner alleges that Koch teaches "depositing a photo resist layer (46) over the layer of metallic germanium (44), exposing and developing the photo resist layer (46) to form a photolithography image (50)". Applicants contend, however, that layer 46 in Koch is not a photo resist layer as is required by claim 11, but is instead an electron-beam sensitive resist (see Koch, col. 5, lines 44-45). Applicants further contend that the layer 46 in Koch is not exposed to light as is required by claim 11, but is instead exposed to an electron beam (see Koch, col. 5, lines 26-29; 46-48).

Based on the preceding arguments, Applicants respectfully maintain that independent claim 11 is not unpatentable over Koch in view of Angelopoulos and Cho and Howe, and that claim 11 is in condition for allowance. Since claims 12, 14, and 36-38 depend from claim 11, Applicants contend that claims 12, 14, and 36-38 are likewise in condition for allowance.

## CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance, and therefore request favorable action. If the Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invite the Examiner to contact Applicants' representative at the telephone number listed below.

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## Appendix A. Identification of Amended Material

Please amend claims 3-6, 8, 11, 14, 19, 21, 26, 28, 30, and 32 as follows:

3. (Amended) A method for etching a semiconductor substrate using a germanium hard mask, the semiconductor substrate having [a] at least one dielectric layer over a major surface thereof, the method comprising the steps of:

a) depositing a layer of metallic germanium over the at least one dielectric layer;

b) patterning the layer of metallic germanium to form the germanium hard mask as a top most layer over the at least one dielectric layer, the patterning step [further] comprising:

i) depositing a photo resist layer over the layer of metallic germanium;

ii) exposing the photo resist layer to light and developing the exposed photo resist layer to form a photolithography image;

iii) etching the layer of metallic germanium through the photolithography image; and

iv) removing the [photoresist] photo resist layer prior to selectively etching the at least one dielectric layer through the germanium hard mask;

c) selectively etching the at least one dielectric layer through the germanium hard mask with the germanium hard mask as a top most layer to form an opening in the at least one dielectric layer; and

d) selectively etching the semiconductor substrate through the opening in the at least one dielectric layer; and

[further comprising the step of] e) [stripping away] removing the layer of metallic germanium after performing the step of selectively etching the at least one dielectric

layer[, the step of stripping away the layer of metallic germanium including the steps of:

oxidizing the layer of metallic germanium to form a layer of germanium oxide therefrom; and

removing the layer of germanium oxide] and before performing the step of selectively etching the semiconductor substrate.

4. ( Amended) The method as claimed in claim [3] 5, the step of removing the layer of germanium oxide including rinsing the semiconductor substrate in water.

5. (Amended) The method as claimed in claim 3, the step of [stripping away] removing the layer of metallic germanium including[stripping away the layer of metallic germanium before performing the step of selectively etching the semiconductor substrate]:

oxidizing the layer of metallic germanium to form a layer of germanium oxide therefrom; and

removing the layer of germanium oxide after performing the step of oxidizing the layer of metallic germanium.

6. (Amended) The method as claimed in claim 3, wherein the step of [depositing a layer of metallic germanium including depositing the layer of metallic germanium having a thickness between approximately 40 nm and approximately 500 nm] oxidizing the layer of metallic germanium. includes heating the semiconductor substrate at elevated temperature in an environment of ambient oxygen.

8. (Amended) The method as claimed in claim 3, further comprising the step of forming [a] the at least one dielectric layer [further] which includes the steps of:

forming a pad oxide layer having a thickness between approximately 5 nm and approximately 30 nm over the major surface of the semiconductor substrate;

depositing a nitride layer having a thickness between 50 nm and approximately 300 nm over the pad oxide layer; and

depositing a mask oxide layer having a thickness between 800 nm and approximately 3,000 nm over the nitride layer.

11. (Amended) A method for fabricating a semiconductor device [having a dielectric stack over a major surface thereof], comprising the steps of:

a) depositing a metallic germanium layer [over the] on a dielectric stack, the dielectric stack having a plurality of dielectric layers disposed on a semiconductor substrate;

b) patterning the metallic germanium layer to form a germanium hard mask as a top most layer over the dielectric stack, the patterning step [further] comprising:

i) depositing a photo resist layer over the metallic germanium layer;

ii) exposing the photo resist layer to light and developing the exposed photo resist layer to form a photolithography image; and

iii) etching the metallic germanium layer through the photolithography image;

c) removing the [photoresist] photo resist layer prior to [selectively] etching the dielectric [layer] stack through the germanium hard mask;

d) etching the dielectric stack through the germanium hard mask with the germanium

hard mask as a top most layer to form a dielectric hard mask over the major surface of the semiconductor substrate;

e) etching the semiconductor substrate through the dielectric hard mask;

f) forming doped regions in the semiconductor substrate; and

g) forming dielectric and conductive structures over the semiconductor substrate; and

[further comprising the step of stripping away] h) removing the metallic germanium layer after the step of etching the dielectric stack and before the step of etching the semiconductor substrate, wherein the step of [stripping away] removing the metallic germanium layer includes the steps of: oxidizing the metallic germanium layer[;], and rinsing the semiconductor substrate in water after performing the step of oxidizing the metallic germanium layer.

14. (Amended) The method as claimed in claim 11, [wherein] further comprising the step of forming [a] the dielectric stack [further] includ[es]ing the steps of:

forming a pad oxide layer having a thickness between approximately 5 nm and approximately 30 nm on the major surface of the semiconductor substrate;

depositing a nitride layer having a thickness between 50 nm and approximately 300 nm on the pad oxide layer; and

depositing a mask oxide layer having a thickness between 800 nm and approximately 3000 nm on the nitride layer.

19. (Amended) A method for etching a semiconductor wafer, [the semiconductor wafer having a

dielectric stack over a major surface thereof, the method] comprising the steps of:

a) forming a germanium hard mask as a top most layer over the dielectric stack, the dielectric stack having a plurality of dielectric layers disposed on a major surface of the semiconductor wafer, the step of forming a germanium hard mask comprising:

depositing a layer of metallic germanium having a thickness equal to or greater than approximately 40nm over the dielectric stack,

depositing a photo resist layer over the layer of metallic germanium [layer],

exposing the photo resist layer to light and developing the exposed photo resist layer to form a photolithography mask, and

etching the layer of metallic germanium through the photolithography mask;

b) removing the [photoresist] photo resist layer prior to [selectively] etching the dielectric [layer] stack through the germanium hard mask;

c) etching the dielectric stack through the germanium hard mask to form a dielectric hard mask over the major surface of the semiconductor wafer; and

d) etching the semiconductor wafer through the dielectric hard mask; and

[wherein the step of forming a germanium hard mask includes the steps of:

depositing a layer of metallic germanium having a thickness equal to or greater than approximately 40nm over the dielectric stack;

patterning the layer of metallic germanium to form the germanium hard mask, and which further includes the steps of:

depositing a photo resist layer over the layer of metallic germanium;

patterning the photo resist layer to form a photolithography mask, and

etching the layer of metallic germanium through the photolithography mask; and further comprising the step of stripping away] e) removing the germanium hard mask after etching the dielectric stack and before etching the semiconductor wafer, wherein the step of [stripping away] removing the germanium hard mask includes the steps of:

oxidizing the layer of metallic germanium to convert the layer of metallic germanium into a layer of germanium oxide[;], and

removing the layer of germanium oxide after performing the step of oxidizing the layer of metallic germanium.

21. (Amended) The method as claimed in claim [3] 19, wherein the step of [patterning the layer of metallic germanium comprises:

depositing a layer of photo resist;

etching the metallic germanium layer through the layer of photo resist; and

removing the layer of photo resist prior to the step of selectively etching the dielectric [layer] stack through the germanium hard mask] oxidizing the layer of metallic germanium. includes heating the semiconductor substrate at elevated temperature in an environment of ambient oxygen.

26. (Amended) A method for etching a semiconductor substrate having [a] at least one dielectric layer over a major surface thereof, the method comprising the steps of:

a) depositing a layer of germanium over the at least one dielectric layer;

b) depositing a [photoresist] photo resist layer over the layer of germanium [layer];

c) exposing the photo resist layer to light and developing the exposed photo resist layer to form a photolithography image;

d) etching the [metallic] layer of germanium [layer] through the photolithography image to form a germanium hard mask over the at least one dielectric layer;

e) removing the [photoresist] photo resist layer from over the germanium hard mask;

f) patterning the at least one dielectric layer through the germanium hard a mask [after removing the photoresist layer from over the germanium hard mask] to form a dielectric hard mask over the semiconductor substrate; and

g) selectively etching the semiconductor substrate through the dielectric hard mask; and

[further comprising the step of stripping away] h) removing the germanium hard mask[ after patterning the at least one dielectric layer to form the dielectric hard mask], [wherein stripping away the layer of germanium] compris[es]ing the steps of: oxidizing the layer of germanium to form a layer of germanium oxide therefrom[;], and removing the layer of germanium oxide after performing the step of oxidizing the layer of metallic germanium.

28. (Amended) The method as claimed in claim 26, wherein [depositing a layer of germanium comprises depositing the layer of germanium having a thickness between approximately 40 nm and approximately 500 nm] oxidizing the layer of germanium includes heating the semiconductor substrate at elevated temperature in an environment of ambient oxygen.

30. (Amended) The method as claimed in claim 26, further comprising forming [a] the at least one dielectric layer by:

forming a pad oxide layer having a thickness between approximately 5 nm and approximately 30 nm over the major surface of the semiconductor substrate;

depositing a nitride layer having a thickness between 50 nm and approximately 300 nm over the pad oxide layer; and

depositing a mask oxide layer having a thickness between 800 nm and approximately 3,000 nm over the nitride layer.

32. (Amended) A method for etching a semiconductor substrate having [a] at least one dielectric layer over a major surface thereof, the method comprising the steps of:

a) depositing a layer of germanium over the at least one dielectric layer;

b) patterning the layer of germanium to form a germanium hard mask, the step further comprising:

i) depositing a photo resist layer over the [metallic] layer of germanium [layer];

ii) exposing the photo resist layer to light and developing the exposed photo resist layer to form a photolithography image;

iii) etching the [metallic ] layer of germanium [layer] through the photolithography image; and

iv) removing the [photoresist] photo resist layer prior to selectively etching the at least one dielectric layer through the germanium hard mask;

c) patterning the at least one dielectric layer through the germanium hard mask using a process selective to germanium to form an opening in the at least one dielectric layer; and

d) selectively etching the semiconductor substrate through the opening in the at least one

dielectric layer[; and

further comprising the step of stripping away the germanium hard mask after patterning the at least one dielectric layer, the step of stripping away the layer of metallic germanium including the steps of:

oxidizing the layer of metallic germanium to form a layer of germanium oxide therefrom; and removing the layer of germanium oxide].